

1000 U.S. PTO
10/081109
03/33/02

U.S. UTILITY Patent Application

PATENT NUMBER and
ISSUE DATE

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10081109	02/25/2002	257	776	2815	Eugene Lee

****APPLICANTS:** Sakamoto Shinsuke; Inbe Yasuo; Yaginuma Masakazu; Horikawa Kazunari; Sei Toshikazu;

****CONTINUING DATA VERIFIED:**
THIS APPLICATION IS A CON OF 09/527,563 03/16/2000

**** FOREIGN APPLICATIONS VERIFIED:**
JAPAN 11-069907 03/16/1999

PG-PUB	DO NOT PUBLISH	<input type="checkbox"/>	RESCIND	<input type="checkbox"/>
Foreign priority claimed		<input checked="" type="checkbox"/> yes <input type="checkbox"/> no	ATTORNEY DOCKET NO	
35 USC 119 conditions met		<input checked="" type="checkbox"/> yes <input type="checkbox"/> no	4329.2270-01	
Verified and Acknowledged Examiners's initials				

TITLE : Semiconductor integrated circuit device and wiring arranging method thereof

U.S. DEPT. OF COMM./PAT. & TM-PTO-436L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G.
		11	1
ISSUE FEE		DRAWING	
Amount Due	Date Paid	Sheets Drwg.	Figs. Drwg.
		2	4
		Print Fig.	1, 2
<input type="checkbox"/> TERMINAL		Applicant's Examiner	
DISCLAIMER		PREPARED FOR ISSUE	
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